Exchange

Von Neumann Architecture - Computer Science



John Von Neumann

- A Hungarian mathematician and physicist.
- A child prodigy able to divide 8 digits in his head.
- Could converse in A
- The Hungarian engineer was known for his mathematical framework and development in functional analysis.
- Developed MANIAC
- Most importantly known for designing the processor architecture.
- Today, his legacy unfolds as his processor is named after him:

The Buses



What is it?

The Von Neumann Architecture started as a concept. This is where a processor would use its control unit in order to process an address of data. Here it would its address for a read access for the data from memory and would be copied back into the control unit.



Bottleneck



Functionality



This architect design is made up of many registers which all process sets data or address between each other.

- 1. The address of the next instruction is copied from the PC to the Memory Address Register (MAR)
- 2. The PC then requests for exchange of the instruction at the address from memory.
- 3. The instruction held at that address is copied to the Memory Data Register (MDR)
- 4. Simultaneously, the contents of the Program Counter (PC) are incremented
- 5. The contents of the MDR are copied to the current Instruction Register (CIR)
- The instruction held in the CIR is decoded.
- 7. It is split into operand and opcode to determine the type of instruction it is. Additional data, if required, is fetched from memory and passed to accumulator.
- 8. The instruction is executed and the result held in accumulator or stored in memorv

Legacy

1

The main legacy of this architecture is that it is now the main basis for many modern computers.

So every time something has been inputted such as the click of a button, the instruction will be exchanged for the data with memory in order to be processed.

Competitors

As intelligence and knowledge over technology increases, vast adjustments of the architecture have been made such as the Harvard architecture which allows 2 memories to be used for less pathways making its data process faster.